AMENDMENTS TO SPECIFICATIONS ARE AS FOLLOWS:

page **1**, paragraphe **2**:

During the fabrication of shallow trench isolation regions in MOSFET devices, the current practice is to sometimes skip depositing a transfer gate sacrificial silicon dioxide layer to decrease the divot (occur at shallow trench corners) depth and improve surface planarity of shallow trench isolation regions during the inherently isotropic wet etch steps. Large divot depths cause leakage problems, particularly for 100 nm node device generation. Ion implantation to form the n- or p- well in these cases is done through the pad oxide. Because of the thickness variations of pad oxide, which may be in the range of 30-50 ~~°A~~ Å, the long channel threshold voltage variation will also be quite large.

page **5**, paragraph **4**:

For the purpose of fabricating a MOSFET device, firstly shallow trench isolation regions are formed as follows: over a semiconductor substrate **10** such as silicon, using chemical vapor deposition (CVD) or plasma-enhanced CVD methods, deposit pad oxide **12** in the range of approximately about 25 – 120 ~~°A~~ Å thick and pad nitride **14** in the range of approximately about 500 – 2000 ~~°A~~ Å thick; using a plasma process, pattern the pad nitride using a resist mask; using nitride as a mask etch into pad oxide and into the silicon substrate to the desired depth of the shallow trench, in the range of approximately about 2000-5000 ~~°A~~ Å using suitable plasma processes known in prior art; fill the shallow trenches with a suitable dielectric material **16** such

as silicon dioxide; planarize the structure using etch-back or preferably chemical mechanical polishing (CMP) method. The resulting structure is shown in Figure 1.

page **6**, paragraph **2**:

After masking the appropriate areas if needed depending on device design (CMOS or MOS), the structure is now exposed to a low energy ion implant beam of As^+ ions: energy of approximately about 3-15 keV, dose of approximately about 5E11-1.5E12, and a tilt angle of approximately about 0-15 degrees. The sacrificial implanted oxide layer **18** (so called because the implanted pad oxide is removed prior to gate formation) is shown in Figure 3. Alternatively B^+ ions are used for forming p- wells. The problem of V_t variation due to pad oxide thickness variation is due to a shift in implantation concentration profile. A TCAD simulation profile using arsenic (As) well implantation is shown in Figure 4 for two pad oxide thicknesses of 50 and 100 ~~°A~~ Å. It is clear from the figure that the shift in implantation profile is due to pad oxide thickness difference. This shift leads to surface As concentration differences, which in turn leads to V_t shift in the device. In order to balance this V_t shift originating from surface concentration shift, a sacrificial shallow implantation is introduced in this invention. Using low energy implantation, dopants are introduced mainly in the pad oxide, while the tail of the profile is inside the silicon substrate as shown in Figure 5. Since the long channel V_t is dependent upon the channel surface concentration, which is decided by the tail of shallow implantation profile at oxide:silicon interface in this case, V_t variation is therefore minimized. The shallow profile concentration in the pad oxide is shown in Figure 5.

page 7, paragraph 2 and Table I:

The V_t values with and without sacrificial shallow implantation are shown in Table I. V_t variation for pad oxide thickness variation in the range of 35 – 110 ~~°A~~ Å is 0.489 +/- 0.0327 volts without shallow sacrificial implantation, whereas it is 0.522 +/- 0.007 volts with shallow sacrificial implantation prior to well implantation.

TABLE I. Threshold Voltage, V_t, for PMOS Device with/without Sacrificial Shallow As^+ Ion Implantation at Various Pad Oxide Thicknesses.

Pad Oxide Thickness, ~~°A~~ Å	110	100	90	80	70	60	35	0
V_t Without Implantation, volts	0.531	0.517	0.503	0.490	0.477	0.465	0.436	0.400
V_t With Implantation, volts	0.520	0.515	0.515	0.520	0.528	0.535	0.522	0.474

page 7/8, paragraph 4/1:

The sacrificial implanted pad silicon dioxide layer **18** is then stripped off in a wet etchant such as dilute hydrofluoric acid which is selective to underlying silicon. Since only one silicon dioxide wet etching step is used, attack of the oxide fill in shallow trenches to form divots, seams, and loss of surface planarity is minimized. The gate dielectric **22** is then grown, as shown in Figure 7. The gate dielectric layer comprises thermally grown or deposited silicon dioxides or

other deposited materials comprising ZrO2, HfO2, and silicates. The gate dielectric layer can be a single layer or a multiple layer stack. Gate dielectric thickness is approximately about 20 – 100 ~~°A~~ Å of equivalent silicon dioxide thickness.